

REMARKS

Claims 174, 176, 177, and 179 stand rejected under 35 U.S.C. § 102(b) as being anticipated by McLaury (U.S. Pat. No.: 5,506,811). Specifically, the Examiner stated:

Note column 2, lines 54+ which discloses the well-known concept of raising the gate voltage of gating transistors during a write operation (boosting the voltage applied to the gates of the FETs so that “the full high logic voltage to be placed on the cell capacitor, since the threshold voltage drop across the gating transistor is eliminated”). Applicant should also note the teachings of the specifically identified patents at lines 57 – 58 of column 2, each of which has been included on the attached PTO-892 form.

It is respectfully submitted that the Examiner has misinterpreted the teachings of McLaury which (in discussing enhancements made to DRAM and VRAM architecture) states that a boosted voltage is applied to a row line attached to the gate of a gating transistor. More specifically, McLaury states:

The first patent [U.S. Pat. No. 4,748,349] describes a circuit which boosts the voltage on the row line and, thus, the gate of the gating transistors to a value above the high logic voltage of the circuit. Boosting permits the full high logic voltage to be placed on the cell capacitor, since the threshold voltage drop across the gating transistor is eliminated.

(Column 2, lines 54 – 63.)

Claim 174 recites “rendering the pair of transistors conductive during a write operation with a control signal that is a boosted version of the voltage used by the array.” Likewise, claims 177 and 179 are amended to recite “said control signal being a boosted version of the voltage used by the array.” In the claimed invention, writing of a full Vdd is accomplished by driving a logic “one” through the isolation transistors; the voltage level of the row lines (i.e., the array voltage) is not boosted. Thus, it is believed that claims 174, 177 and 179 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 174, 177, and 179 pursuant to 35 U.S.C. §102(b) be withdrawn.

Claims 175 and 176, claim 178, and claims 180 and 181 depend from allowable base claims 174, 177, and 179 respectively. For the reasons discussed above in conjunction with claims 174, 177, and 179, it is believed that claims 175, 176, 178, 180, and 181 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 175, 176, 178, 180, and 181 pursuant to 35 U.S.C. § 102(a) be withdrawn.

Claims 175, 178, 180, and 181 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McLaury. Specifically, the Examiner stated:

Appl. No.: 09/934,795
Docket No.: DB000575-023
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These claims, reciting a specific amount of boosting of the gate voltage (i.e., $V_{cc} + V_{th}$) do not distinguish patentably over McLaury's teachings because those having ordinary skill in the art will easily recognize that, in order to remove the V_{th} drop (gate-source), it is simply necessary to raise the gate voltage by V_{th} above the standard logic "1" voltage of the write circuitry. This does not constitute patentable difference over McLaury.

As discussed above, claims 175, 178, and 180 – 181 depend from allowable base claims 174, 177, and 179 respectively. Thus for the same reasons discussed above in conjunction with claims 174, 177, and 179, it is believed that claims 175, 178, and 180 – 181 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 175, 178, and 180 – 181 pursuant to 35 U.S.C. § 103(a) be withdrawn.

Applicants have made a diligent effort to place the claims in condition for allowance. Accordingly, a Notice of Allowance for claims 174 - 181 is respectfully requested. If the Examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the Examiner is respectfully requested to contact applicants' attorney at the telephone number listed below so that additional changes may be discussed.

Respectfully submitted,



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